CLAIMS

1. An RF circuit (RFCT) comprising:
- a voltage controlled oscillator (VCO) delivering an RF signal (V1, F1),
- a phase locked loop (PLL) to control the voltage controlled oscillator (VCO),
- a modulation circuit (TXCT) receiving the RF signal (V1, F1) and delivering a modulated signal (RFSx) comprising at least one harmonic component (H1, H2, H4) of a frequency equal or proximate to that of the RF signal delivered by the voltage controlled oscillator, the harmonic component being capable of disturbing the operation of the voltage controlled oscillator by injection pulling,

characterised in that it comprises:
- an injection pulling compensation circuit (COMPCT, COMPCT1, COMPCT2, COMPCT3), comprising one input receiving at least the disturbing harmonic component (H1, H2, H4) and means for modifying the phase and the amplitude of the harmonic component to deliver an injection pulling compensation signal (Bcomp), and
- means for injecting the compensation signal (Bcomp) into the voltage controlled oscillator.

2. RF circuit according to claim 1, wherein the compensation circuit (COMPCT, COMPCT1, COMPCT2, COMPCT3) is amplitude and phase adjusted such that the compensation signal injected into the voltage controlled oscillator has an amplitude substantially equal to the amplitude of a spurious signal (Anet) resulting from the involuntary injection into the voltage controlled oscillator, by at least one spurious path (SA1, SA2, SA3... SAn), of the disturbing harmonic component, and a phase opposite that of the spurious signal.

3. RF circuit according to one of claims 1 and 2, wherein the compensation circuit (COMPCT1) is a single ended circuit that delivers a compensation signal having a unique component that is injected at one point of the voltage controlled oscillator.

4. RF circuit according to one of claims 1 and 2, wherein the compensation circuit (COMPCT2) is a single ended circuit that delivers a compensation signal having two components (Bcomp1, Bcomp2) that are injected at two different points of the voltage controlled oscillator.

5. RF circuit according to one of claims 1 and 2, wherein the compensation circuit (COMPCT3) is a balanced circuit that delivers a compensation signal having two components (Bcomp1', Bcomp2') in opposite phase that are injected at two different points of the voltage controlled oscillator.

6. RF circuit according to one of claims 1 to 5, wherein the compensation circuit receives at input a harmonic component (H2, H4) taken off in the modulation circuit.

7. RF circuit according to claim 6, wherein the compensation circuit receives at input a harmonic component (H2, H4) taken off in an output amplifier (RFAMP) of the modulation circuit.

8. RF circuit according to one of claims 1 to 5, wherein the compensation circuit receives at input a harmonic component delivered by a harmonic generating circuit distinct from the modulation circuit.

9. RF circuit according to one of claims 1 to 8, wherein the compensation circuit comprises a phase-shift

circuit (PSN) to modify the phase of the harmonic component received at input.

10. RF circuit according to one of claims 1 to 8, wherein the compensation circuit comprises a phase-shift circuit (QGEN1) receiving the disturbing harmonic component and delivering two phase quadrature signals.

11. RF circuit according to one of claims 1 to 8, wherein the compensation circuit comprises a phase-shift circuit (QGEN2) receiving the disturbing harmonic component and delivering phase quadrature and opposite phase signals.

12. RF circuit according to claim 11, wherein the phase-shift circuit (QGEN2) comprises a balanced bridge of resistors and capacitors that is quite insensitive to the temperature.

13. RF circuit according to one of claims 1 to 12, wherein the compensation circuit (COMPCT, COMPCT1, COMPCT2, COMPCT3) comprises at least one attenuator circuit (ATTC, IAT1, IBAT1, QAT1, QBAT1, IAT2, IBAT2, QAT2, QBAT2) to modify the amplitude of the harmonic component received at input.

14. RF circuit according to claim 13, wherein the attenuator circuit comprises adjustable resistors or capacitors or a combination of these elements.

15. RF circuit according to claim 13, comprising a group of at least two attenuator circuits (IAT1, IBAT1, QAT1, QBAT1, IAT2, IBAT2, QAT2, QBAT2) the outputs of which are added up to control the phase and the amplitude of the compensation signal.

16. RF circuit according to claim 15, comprising a group of attenuator circuits (IAT1/QAT1, IBAT1/QBAT1) having their outputs added up and receiving at input phase quadrature signals coming from the disturbing harmonic component.

17. RF circuit according to claim 15, comprising a group of attenuator circuits (IAT2/IBAT2/QAT2/QBAT2) having their outputs added up and receiving at input phase quadrature and opposite phase signals coming from the disturbing harmonic component.

18. RF circuit according to one of claims 15 to 17, wherein an attenuator circuit (IAT1, IBAT1, QAT1, QBAT1, IAT2, IBAT2, QAT2, QBAT2) comprises electrically adjustable capacitors or electrically adjustable resistors, which are adjusted by analog signals delivered by a digital to analog converter.

19. RF circuit according to claim 18, wherein digital data for adjusting the capacitors of the attenuator circuit are stored in memory cells (NVREG) and are applied to the digital to analog converter.

20. RF circuit according to one of claims 1 to 19, wherein the compensation signal (Bcomp) is injected onto one terminal of an active component (T1, T2) of the voltage controlled oscillator.

21. RF circuit according to one of claims 1 to 19, wherein the compensation signal (Bcomp) is injected onto one terminal of a passive component (C1, C2) of the voltage controlled oscillator.

22. RF circuit according to one of claims 1 to 19, wherein the means for injecting the compensation signal

(Bcomp) comprise an injection inductor (Lc) coupled to an inductor (L1) of the voltage controlled oscillator.

23. A method for stabilising the operation of a voltage controlled oscillator (VCO) driven by a phase locked loop (PLL), the voltage controlled oscillator delivering an RF signal (V1, F1) and receiving through at least one spurious path a harmonic component (H1, H2, H4) of a frequency equal or proximate to that of the RF signal sent, capable of disturbing the operation of the voltage controlled oscillator by injection pulling,

characterised in that it comprises the injection, into the voltage controlled oscillator, of an injection pulling compensation signal (Bcomp), the phase and the amplitude of which are adjusted so as to neutralise the disturbing effects of the harmonic component.

24. Method according to claim 23, wherein the compensation signal is amplitude and phase adjusted so as to have an amplitude substantially equal to the amplitude of a spurious signal (Anet) resulting from the involuntary injection into the voltage controlled oscillator, by at least one spurious path (SA1, SA2, SA3... SAn), of the disturbing harmonic component, and a phase opposite that of the spurious signal.

25. Method according to one of claims 23 and 24, comprising the single ended injection, at one point of the voltage controlled oscillator, of a compensation signal having a unique component.

26. Method according to one of claims 23 and 24, comprising the injection of a compensation signal having two components (Bcomp1, Bcomp2), and the single ended injection of these components at two different points of the voltage controlled oscillator.

27. Method according to one of claims 23 and 24, comprising the injection of a compensation signal having two components (Bcomp1', Bcomp2') in opposite phase, and the injection of these two components at two different points of the voltage controlled oscillator.

28. Method according to one of claims 23 to 27, wherein the compensation signal is generated from at least one harmonic component (H1, H2, H4) taken off in the modulation circuit.

29. Method according to claim 28, wherein the compensation signal is generated from at least one harmonic component (H2, H4) taken off in an amplifier (RFAMP) of a modulation circuit from which the disturbing harmonic component is sent.

30. Method according to one of claims 23 to 29, wherein the compensation signal is generated from one harmonic component produced by a harmonic generating circuit.

31. Method according to one of claims 23 to 30, wherein the phase of the compensation signal is adjusted by means of a phase-shift circuit (PSN).

32. Method according to claim 31, wherein the amplitude of the compensation signal is adjusted by means of an attenuator circuit (ATTC) comprising adjustable resistors or capacitors or a combination of these elements.

33. Method according to one of claims 23 to 30, wherein the amplitude and the phase of the compensation signal are adjusted by means of a group of at least two attenuator circuits (IAT1, IBAT1, QAT1, QBAT1, IAT2, IBAT2, QAT2, QBAT2) the outputs of which are added up.

34. Method according to claim 33, wherein the amplitude and the phase of the compensation signal are adjusted by means of a group of attenuator circuits (IAT1/QAT1, IBAT1/QBAT1) having their outputs added up and receiving at input phase quadrature signals coming from the disturbing harmonic component.

35. Method according to claim 33, wherein the amplitude and the phase of the compensation signal are adjusted by means of a group of attenuator circuits (IAT2/IBAT2/QAT2/QBAT2) having their outputs added up and receiving at input phase quadrature and opposite phase signals coming from the disturbing harmonic component.

36. Method according to claim 35, wherein the phase quadrature and opposite phase signals are generated by means of a phase-shift circuit comprising a balanced bridge of resistors and capacitors that is quite insensitive to the temperature.

37. Method according to one of claims 33 to 35, wherein an attenuator circuit (IAT1, IBAT1, QAT1, QBAT1, IAT2, IBAT2, QAT2, QBAT2) comprises electrically adjustable capacitors or electrically adjustable resistors that are adjusted by analog signals coming from adjustment digital data.

38. Method according to claim 37, wherein the adjustment digital data are stored in memory cells (NVREG).

39. Method according to one of claims 23 to 38, wherein the compensation signal (Bcomp) is injected onto one terminal of an active component (T1, T2) of the voltage controlled oscillator.

40. Method according to one of claims 23 to 38, wherein the compensation signal (Bcomp) is injected onto one terminal of a passive component (C1, C2) of the voltage controlled oscillator.

41. Method according to one of claims 23 to 38, wherein the compensation signal (Bcomp) is injected by inductive coupling.